IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: TI-25711.1

Stephen Hsiao-Yi Li, et al. Art Unit:

Serial No: Examiner:

Filed: April 6, 2001

For: Data Processing Device With an Indexed Immediate Addressing Mode

PRELIMINARY AMENDMENT

EXPRESS MAILING" Mailing Label No. **EL547742401.** Date of Deposit: **April 6, 2001.** I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown above and is addressed to: Ass't Commissioner for Patents, Washington, D.C. 20231.

Robin E. Barnum

Ass't Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to examination of the above-identified patent application, please amend as follows:

IN THE SPECIFICATION:

Page 1, after the title, but before Line 1 insert:

--This is a division of application Serial No. 08/851,573, filed May 2, 1997.--

Page 4, line 27: delete "method", second occurrence;

Page 12, line 11: replace "_____, (U.S. Patent)" with --5,644,310--;

Line 12: delete "Application Serial No. 08/475,251"; and

Line 13: replace "Application Serial No. 08/054,768" with --5,657,423--.

IN THE CLAIMS:

Please cancel Claims 1-12, and amend Claim 13 as follows:

13. (Amended) An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal;

a digital to analog converter connected to the output terminal operable to convert the channel of PCM data to an analog audio signal on a D/A output terminal;

a speaker subsystem connected to the D/A output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

Please add new Claims 17-25, as follows:

--17. The system of Claim 13, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

18. The system of Claim 13, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

19. The system of Claim 18, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

20. The system of Claim 19, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.

21. An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

22. The system of Claim 21, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

23. The system of Claim 21, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

24. The system of Claim 23, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

25. The system of Claim 24, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.--

REMARKS

The parent application originally presented Claims 1-16. The Examiner of the parent application required a restriction to group I, Claims 1-12 or to Group II, Claims 13-16. The Applicant elected group I with traverse, which was denied. This

divisional reasserts group II. Claims 1-12 from the parent application are canceled. Claims 17-25 have been added in this Preliminary Amendment. Claims 13-25 are pending in the present application.

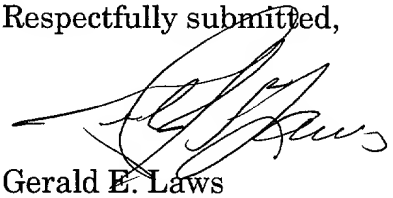
Claim 13 is amended to comport with allowed Claim 1 of the parent application. New Claims 17-20 comport with allowed Claims 2-5 of the parent application. New Claims 21-25 are now presented in order to more fully protect the inventors' contribution to the art.

A typographical correction has been made to the specification, as well as updating of various referred to Serial Numbers, which are now patents. No new matter has been added.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

13. (Amended) An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal;

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a speaker subsystem connected to the D/A output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

Please add new Claims 17-25

--17. The system of Claim 13, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field

as a most significant address portion with the first portion of the first address as a least significant address portion.

18. The system of Claim 13, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

19. The system of Claim 18, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

20. The system of Claim 19, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.

21. An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field

selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

22. The system of Claim 21, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

23. The system of Claim 21, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

24. The system of Claim 23, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

25. The system of Claim 24, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.--